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DATA SHEET

SAA2510
Video CD (VCD) decoder

Preliminary specification
File under Integrated Circuits, IC02

1996 May 21

Philips
Semiconductors

PHILIPS

Video CD (VCD) decoder SAA2510

FEATURES

(With standard microcode loaded)

- Decoding and display of MPEG1 video streams (constrained parameters)
- Decoding of MPEG audio streams (layer II)
- Decoding, storage (compressed) and display of high-resolution still pictures of 704 × 576 pixels
- Requires only 4 Mbits of external 70 ns DRAM
- Audio transparency mode for CD-DA discs
- On-screen display capability
- Play options:
  - Play
  - Stop
  - Pause/continue
  - Slow-motion forward
  - Scan forward
  - Scan backward.
- Supports auto-pause feature
- Disc interface: Philips I²S, EIAJ, MEC formats and IEC 958 (EBU) interface
- Separate error flag input (EFIN) and data valid input (NDAV)
- Performs basic block decoder functions:
  - serial-to-parallel conversion
  - sync detection
  - descrambling
  - EDC calculation
  - error-correction for mode 2 form 1 sectors
  - header and sub-header interpretation.
- I²C-bus interface
- Video output YUV 4 : 2 : 2 format. DMSD bus compatible
- Also supports CCIR656 video interface, including line and field timing codes
- Audio output: 44.1 kHz. 16, 18 or 20 bits per audio sample in Philips I²S, Sony or MEC formats
- EBU audio output, fully transparent from input to output in CD-DA mode and generated in MPEG mode
- Downloadable microcode for internal controllers
- Internal video timing generator
- Requires 40 MHz crystal for system clock generation
- Requires 27 MHz crystal or external 27 MHz source for video timing generation
- Requires 16.9344 MHz (384 × 44.1 kHz) clock locked to CD drive
- Internal generation of 90 kHz MPEG clock
- Capability of sharing external DRAM by 3-stating all DRAM pins.

APPLICATION

- Dedicated video CD players.

GENERAL DESCRIPTION

MPEG1 audio and video CD (VCD) decoder, intended for use in low-cost dedicated video CD players. When used with a 4 Mbit DRAM and a digital video encoder, the decoder adds the required functionality to a CD decoder to implement a low-cost video CD player capable of playing discs coded to version 2.0 of the video CD specification. The SAA2510 is an I²C-bus controlled chip and features serial data input in four common bus formats. It provides digital video output in CCIR601 and 656 formats.

A bit-mapped on-screen display is provided and output video timing can be 525 lines/30 frames per second or 625 lines/25 frames per second. The chip is microcode programmable for feature enhancement.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2510	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT317-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD3}	supply voltage	3.0	3.3	3.6	V
V_{DD5}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	tbf	–	mA
$f_{xtal\ s}$	system clock crystal frequency	–	40.0	–	MHz
$f_{xtal\ v}$	video clock crystal frequency	–	27.0	–	MHz
f_i	audio clock input frequency	–	16.9344	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

BLOCK DIAGRAM

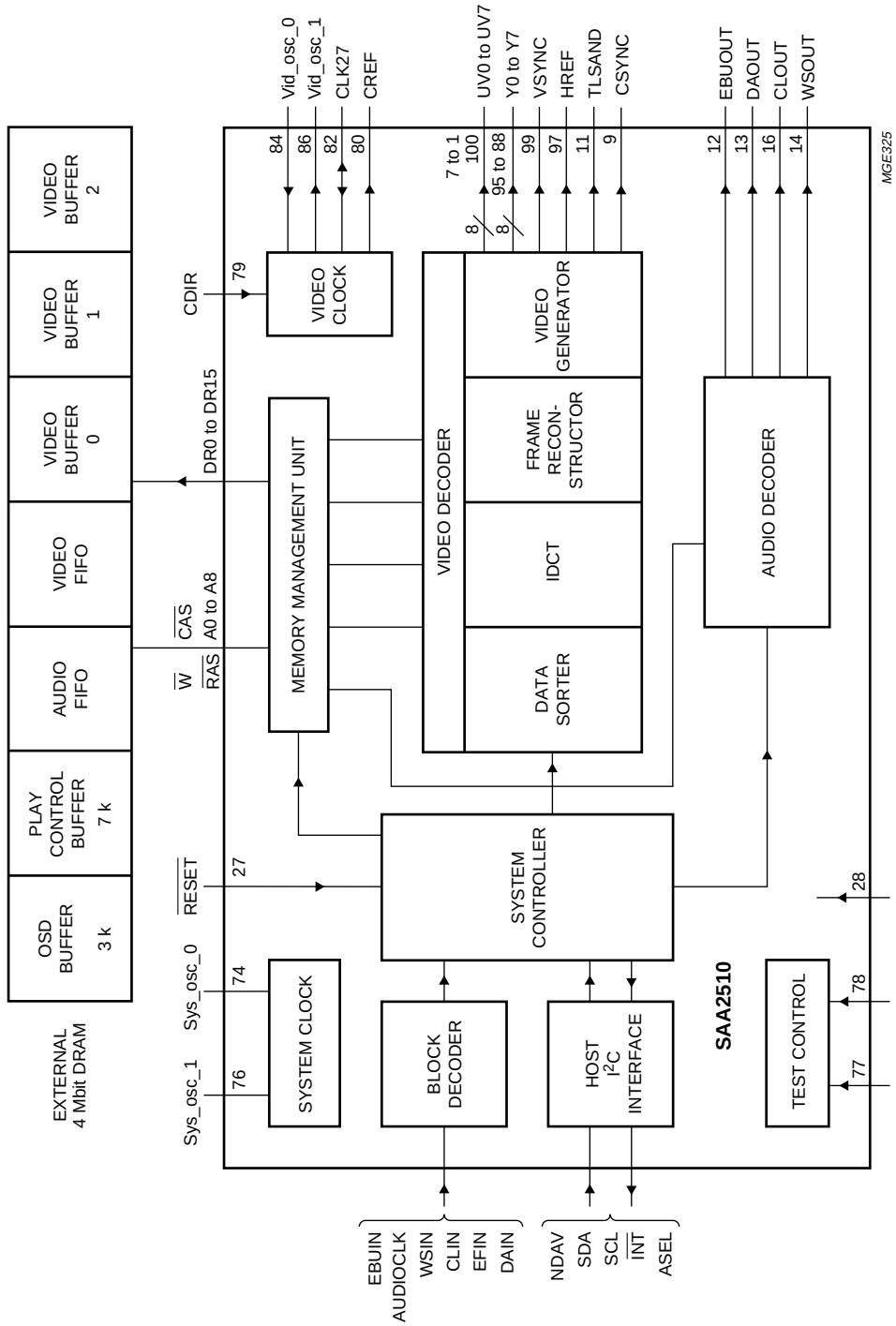


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
UV6	1	video UV bus output bit 6; 16-bit video output mode: the UV bus outputs alternating U and V chroma samples at 13.5 Mbytes/s CCIR656 mode: this bus is not used (inactive)
UV5	2	video UV bus bit 5
UV4	3	video UV bus bit 4
UV3	4	video UV bus bit 3
UV2	5	video UV bus bit 2
UV1	6	video UV bus bit 1
UV0	7	video UV bus bit 0
V_{DD5}	8	5 V external pad power supply
CSYNC	9	composite sync output; 525 lines/60 Hz or 625 lines/50 Hz
V_{SS5}	10	0 V external pad power supply
TLSAND	11	two-level Sandcastle (composite blanking) output; requires external resistor network to define horizontal/vertical blanking level
EBUOUT	12	IEC 958 digital audio output
DAOUT	13	I^2S data; digital audio output
WSOUT	14	I^2S word select digital audio output
V_{DD3}	15	+3 V internal power supply
CLOUT	16	I^2S bit clock output
V_{SS}	17	0 V internal power supply
AUDIOCLK	18	16.9 MHz audio clock input
V_{DD5}	19	5 V internal power supply
EBUIN	20	EBU (IEC 958) input
CLIN	21	I^2S bit clock input
WSIN	22	I^2S word select input
DAIN	23	I^2S digital data input
V_{DD3}	24	+3 V internal power supply
EFIN	25	error flag input from I^2S source
V_{SS}	26	0 V internal power supply
$\overline{RESET}$	27	active low reset input
DRAMON	28	DRAM pin 3-state control input; also 3-states video outputs and some timing signals
$\overline{INT}$	29	active low open drain interrupt request to host microcontroller
NDAV	30	data not valid input (data on I^2S or EBU input not valid)
ASEL	31	I^2C-bus address select pin
SDA	32	I^2C-bus data pin
V_{DD5}	33	5 V external pad power supply
SCL	34	I^2C-bus clock input
V_{SS5}	35	0 V external pad power supply
DR15	36	DRAM data input/output bit 5

SYMBOL	PIN	DESCRIPTION
DR14	37	DRAM data input/output bit 14
DR13	38	DRAM data input/output bit 13
DR12	39	DRAM data input/output bit 12
DR11	40	DRAM data input/output bit 11
DR10	41	DRAM data input/output bit 10
DR9	42	DRAM data input/output bit 9
V_{DD5}	43	5 V external pad power supply
DR8	44	DRAM data input/output bit 8
V_{SS5}	45	0 V external pad power supply
DR7	46	DRAM data input/output bit 7
DR6	47	DRAM data input/output bit 6
DR5	48	DRAM data input/output bit 5
DR4	49	DRAM data input/output bit 4
DR3	50	DRAM data input/output bit 3
DR2	51	DRAM data input/output bit 2
DR1	52	DRAM data input/output bit 1
DR0	53	DRAM data input/output bit 0
V_{SS5}	54	0 V external pad power supply
$\overline{CAS}$	55	DRAM column address strobe
V_{DD5}	56	5 V external pad power supply
A8	57	DRAM row/column address pin A8
A7	58	DRAM row/column address pin A7
A6	59	DRAM row/column address pin A6
A5	60	DRAM row/column address pin A5
A4	61	DRAM row/column address pin A4
V_{DD3}	62	+3 V internal power supply
$\overline{W}$	63	active low DRAM write strobe
V_{SS}	64	0 V internal power supply
$\overline{RAS}$	65	DRAM row address strobe
V_{DD5}	66	5 V internal power supply
A3	67	DRAM row/column address pin A3
V_{SS5}	68	0 V external pad power supply
A2	69	DRAM row/column address pin A2
V_{DD5}	70	5 V external pad power supply
A1	71	DRAM row/column address pin A1
A0	72	DRAM row/column address pin A0
V_{DDO3}	73	3 V internal power supply for oscillator
Sys_osc_0	74	oscillator input pin; 40 MHz oscillator
V_{SS}	75	0 V internal power supply
Sys_osc_1	76	oscillator output pin; 40 MHz oscillator
TP1	77	factory test pin; connect to ground

SYMBOL	PIN	DESCRIPTION
TP2	78	factory test pin; connect to ground
CDIR	79	clock direction control pin; when high, CLK27 is an output
CREF	80	clock qualifier output; 13.5 MHz timing signal used in 16-bit video output mode; can also be used as 13.5 MHz video sample clock
V_{SS5}	81	0 V external pad power supply
CLK27	82	27 MHz clock input or output; direction controlled by CDIR pin
V_{DD5}	83	5 V external pad power supply
Vid_osc_0	84	oscillator pin; 27 MHz; input pin
V_{SS}	85	0 V internal power supply
Vid_osc_1	86	oscillator pin; 27 MHz; output pin
V_{DDO3}	87	3 V internal power supply for oscillator
Y7	88	video Y bus output bit 7 DMSD mode: the Y bus outputs luminance samples at 13.5 Mbytes/s CCIR656 mode: this pin supplies multiplexed chrominance and luminance (27 Mbytes/s)
Y6	89	video Y bus bit 6
Y5	90	video Y bus bit 5
Y4	91	video Y bus bit 4
Y3	92	video Y bus bit 3
Y2	93	video Y bus bit 2
Y1	94	video Y bus bit 1
Y0	95	video Y bus bit 0
V_{SS5}	96	0 V external pad power supply
HREF	97	horizontal (line) timing reference signal; high during active video part of line, low during line blanking
V_{DD5}	98	5 V external pad power supply
VSYNC	99	vertical (field/frame) timing reference signal; high during vertical blanking interval of field
UV7	100	video UV bus output bit 7 DMSD mode: the UV bus outputs alternating U and V chroma samples at 13.5 Mbytes/s CCIR656 mode: this bus is not used (inactive)

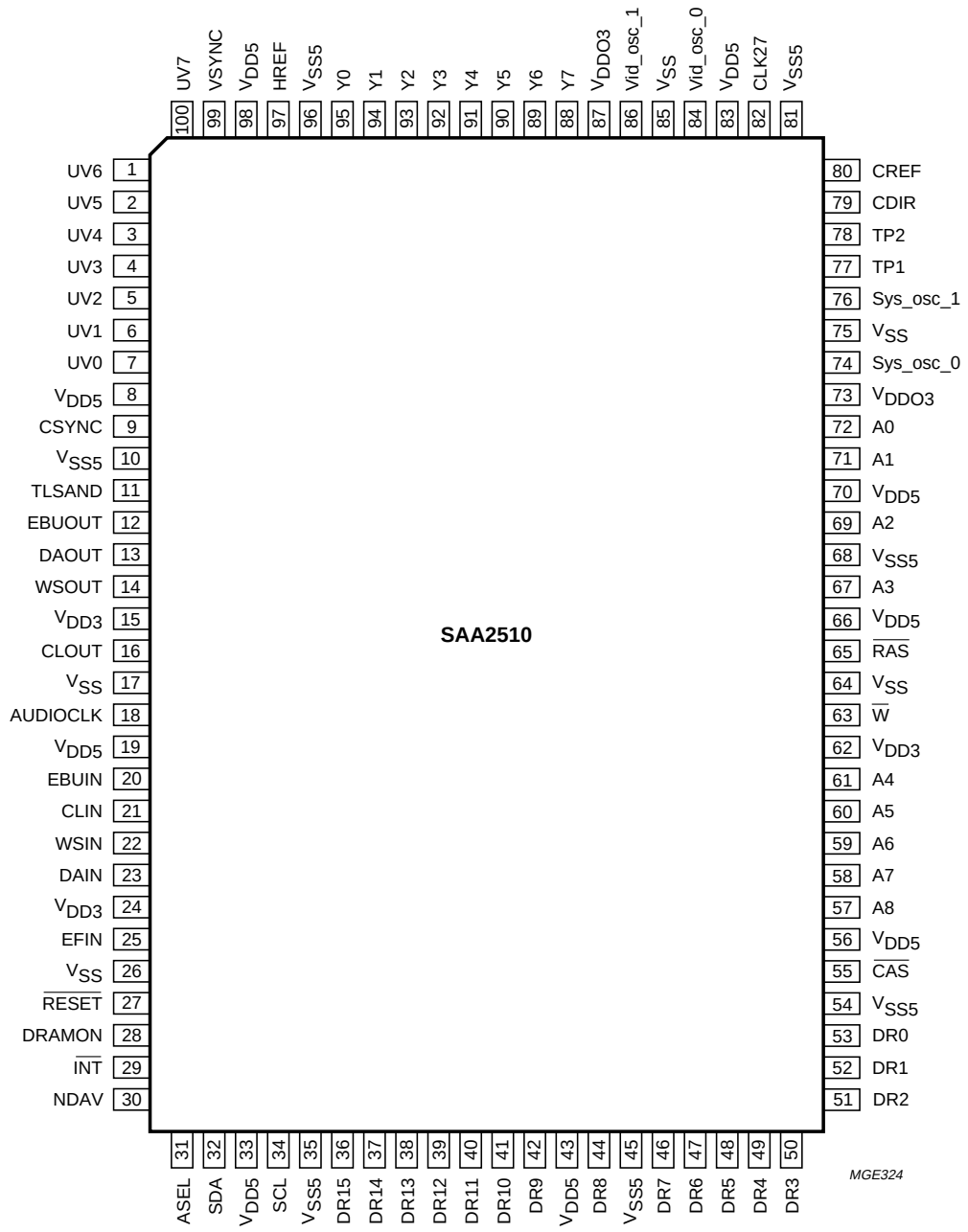


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Block decoder

The VCD chip receives MPEG A/V or CD digital audio data from a CD decoder chipset using any one of four common interface formats (Philips I²S, EIAJ, MEC or IEC 958). The Philips I²S, EIAJ and Matsushita input modes use the bit clock (CLIN), word select (WSIN), data (DAIN) and error flag (EFIN) inputs. If IEC 958 (EBU) input mode is selected, only the EBUIN pin needs to be connected. The chip also requires a 16.9 MHz clock input (CLIN) which is synchronous with the data input from the CD decoder providing the serial data input.

The VCD chip contains a block decoder and descrambler which performs error correction on the Video CD data track (form 1) sectors and error detection on real-time audio and video tracks where an error correction code is present.

In most events, audio output can be in any of the three (I²S, EIAJ or MEC) formats, independent of input type. When playing CD digital audio discs, the input is copied to the outputs.

The block decoder supports some special functions which enable recovery of play control lists. The desired sectors can be acquired by programming a sector address via the I²C-bus microcontroller interface. The microcontroller then instructs the CD servo/decoder subsystem to execute a servo jump to the required disc location and then waits for an interrupt indicating that the desired sector information has been received and error-corrected.

System controller

Overall control of the chip and a number of its less time-critical functions is carried out by a dedicated RISC processor. The microcode for this processor is executed from an on-chip RAM. This microcode must be loaded into RAM after power-up by the host microcontroller, using the I²C-bus interface. This enables the functionality of the chip to be customized for specific applications.

On-screen display

The VCD chip provides a bit-mapped On-Screen-Display (OSD), containing 32 display lines of 352 pixels per line. There is a double-height mode which repeats OSD lines so that the maximum height of OSD objects becomes 64 lines. This character-set-independent OSD permits display of ideographic characters and simple graphic displays anywhere on the screen.

The OSD is implemented as 48 vertical ‘slices’ of 8 pixels (horizontally) and 32 (vertically). Each pixel is stored as 2 bits. This gives three programmable logical colours, plus a transparent option. Each slice is identified by a slice code (slice number).

The horizontal position of a slice is defined by its position in a slice code sequence written to the VCD chip. This arrangement reduces the need to completely update the OSD bit map in many situations. It may be possible to simply reorder the slices, e.g. if a track time display is being updated and slices are prepared to represent digits. At any time, up to 44 of the 48 slices can be displayed.

Video decoder

Video output data can be presented in one of two modes:

1. 16-bit wide data is output in YUV 4 : 2 : 2 format as 8 bits of luminance and 8 bits of alternating U and V chrominance. The video output data rate in this mode is 13.5 Mwords/s.
2. 8-bit wide, CCIR656-like, data is output providing 4 : 2 : 2 format video as an 8-bit UYVY multiplex at 27 Mbytes/s.

In either case, the VCD chip can be programmed to output 525 line or 625 line format timing to match the type of display (TV) connected to its output. Additional programmability is provided to cope with the Video CD disc source picture coding type (525/625 lines).

The VCD chip performs vertical and horizontal interpolation to convert the MPEG SIF (352 pixels per line) normal resolution pictures to CCIR601 resolution. Vertically interpolated pixels are output on the odd fields during display of normal resolution pictures.

The Video CD disc being played may have been coded with 525 lines/60 Hz or 625 lines/50 Hz pictures. When the Video CD player is connected to a display with a different timebase to the coded disc material, some adjustments must be made to allow for the different number of lines on the display and the reconstructed picture. Two examples are shown in Figs. 3 and 4.

The VCD chip can be programmed to position the reconstructed picture with respect to horizontal and vertical syncs anywhere on the display screen with a programmable ‘viewport’ position. Figure 3 shows an MPEG SIF resolution picture (352 pixels by 288 lines) being displayed on an NTSC display having only 240 active display lines per field. In this event, the top and bottom 24 lines are not displayed.

The second example, illustrated in Fig.4, is where a 240 active lines per field NTSC picture needs to be displayed on a 288 line PAL format display. The ‘missing’ lines can be filled with a programmable border colour.

High-resolution still pictures can be present on a Video CD disc.

In this event, the horizontal and vertical resolution of the reconstructed picture is double that of normal resolution (moving) pictures. In order to fit the picture in the available frame buffer DRAM, a data compression scheme is applied to the stored picture.

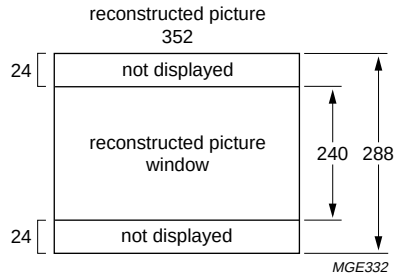


Fig.3 One field of a 625-line picture on a 525-line display.

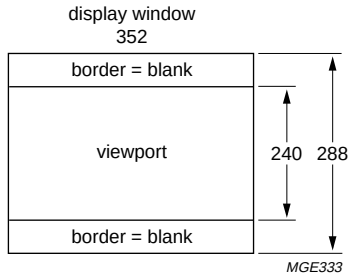


Fig.4 525-line picture on a 625-line display.

‘Trickmode’ implementation

Compared with CD digital audio players, it is likely that Video CD players will need to offer additional functionality similar to VCRs. These features are commonly called ‘trickmodes’. Typically, the player will offer features such as still picture (freeze frame), scan forwards and backwards as well as slow motion replay.

These features require a combination of CD servo control and Video CD decoder functions for effective implementation. The VCD chip provides high level command features to support these modes in order to minimize microcontroller time-critical software.

STILL PICTURE DISPLAY

This is implemented directly using a Pause command, causing the VCD chip to hold the displayed picture at the next frame update.

SCAN FORWARD AND SCAN BACKWARDS

There is no difference as far as the VCD chip is concerned. The controlling microcomputer must command the CD servo to execute a servo jump and re-synchronize. The VCD chip is then commanded to display the next I (Intra-coded) picture following re-acquisition of sector sync.

SLOW-MOTION REPLAY

A command is provided by the VCD chip, allowing a slow-motion ‘factor’ in the range 2 to 8 to be selected. This is the factor by which replay will be slowed down. Because the rate of decoding of video sectors has been reduced, the video FIFO fills up. The block decoder is designed to automatically disable acquisition when the video FIFO fills in this way and an interrupt is generated. At this point, the next wanted sector (address) has been loaded into a register in the VCD chip. The controlling microcomputer then commands a CD servo jump to position on the disc just before the next desired sector, making allowance for re-synchronization by the servo and VCD chip.

I²C-bus interface

The VCD chip is programmed via the I²C-bus interface. The chip is a slave transceiver capable of operating at the maximum specified bus clock frequency of 400 kHz. It does not support the general call feature. One of two slave addresses can be used. The address is selected by the ASEL input pin.

This bus provides access to the internal registers of the device. The bus is also used to write OSD slice data and to read data stored in three play-control sector buffers, which normally will be used to store Video CD data track information. This interface features a two or three byte sub-addressing scheme allowing access to any DRAM location. However, in normal use, only two byte sub-addressing is needed.

An interrupt pin is available to signal a number of events so that the controlling processor does not need to poll VCD status registers.

Input pin NDAV is used to signal that data on the block decoder input is not valid, e.g. during CD servo jumps.

A complete memory map and list of registers will be included in a later version of this data sheet.

I²C-bus slave address selection

A6	A5	A4	A3	A2	A1	A0	R/W
0	0	1	1	0	1	A0[1]	

Note

1. ASEL.

The data transfer protocol is as follows:

Two and three byte sub-addressing: first the device sub-address is transmitted, preceded by a START condition and the slave address:

Two and three byte sub-addressing

S	SLA	W	SUB_A
S = START			
SLA = Slave address			
W = Write			
SUB_A = Sub-address			

The sub-address can be either 2 or 3 bytes. The 3-byte sub-address is used for DRAM random access. This is not used for normal operation. It exists only as a test mode. Since the Video CD IC is internally fully word (16 bits) oriented, the sub-address must always be an even address. If an odd-numbered address is given, the Video CD IC will not acknowledge this byte. For the sub-address, the least significant byte is sent first. The second sub-address byte contains 2 control bits.

Sub-address byte format

MSB							LSB	MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0	C1	C0	A13	A12	A11	A10	A9	A8

When A0 is a '1', the address byte is not acknowledged (odd address).

Explanation of control bits

C0 = 0; 2-byte sub-address.

C0 = 1; 3-byte sub-address. The next byte transmitted is also an address byte:

3-byte sub-address - most significant byte format

MSB							LSB
0	0	0	A18	A17	A16	A15	A14

C1 = 0; sub-address post increment enabled. After each transfer of 2 bytes, the address is automatically incremented by 2.

C1 = 1; sub-address post increment disabled.

The master will terminate a read action by NOT acknowledging the last read byte followed by a STOP condition.

I²C-bus transaction summary

The following notation is used to describe bus transactions:

S: START condition generated by bus master

P: STOP condition generated by bus master

A: Acknowledge bit generated by master or slave according to transaction type and stage

N: Negative acknowledge; acknowledge bit is not set by bus master during last byte of a read

SLA: 7-bit slave address generated by bus master

W: R/W bit after slave address is set to write

R: R/W bit after slave address is set to read

SUB_N: Sub-address byte N (N = 0, 1 or 2); least significant address byte is SUB_0

D(M): A data byte transmitted by master or slave on the bus; D(0) is the first byte sent; as all transfers must be an even number of bytes, it follows that M must be odd.

Set 2-byte sub-address and write (M + 1) bytes

S	SLA	W	A	SUB_0	A	SUB_1	A	D(0)	A	D(1)	A to D(M)	A	P

Set 2-byte sub-address and read (M + 1) bytes

S	SLA	W	A	SUB_0	A	SUB_1	A	S	SLA	R	D(0)	A	D(1)	A to D(M)	N	P

Set 3-byte sub-address and write (M + 1) bytes

S	SLA	W	A	SUB_0	A	SUB_1	A	SUB_2	A	D(0)	A	D(1)	A to D(M)	A	P

Set 3-byte sub-address and read (M + 1) bytes

S	SLA	W	A	SUB_0	A	SUB_1	A	SUB_2	A	S	SLA	R	A	D(0)	A	D(1)	A to D(M)	N	P

This addressing mode is valid only if sub-address auto incrementing is disabled. It is intended for fast polling of a status register.

Byte-order within words

	LSB															MSB
Word	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
I^2C-bus	B7	B6	B5	B4	B3	B2	B1	B0	B15	B14	B13	B12	B11	B10	B9	B8

For each transmitted word (read or written) the least significant byte is transmitted first.

CHARACTERISTICS

T_{amb} = –20 to +70 °C; V_{DD5} = 4.5 to 5.5 V; V_{DD3} = 3.0 to 3.6 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD5}	supply voltage (5 V) range		4.5	5	5.5	V
I_{DD5}	V_{DD5} supply current		–	tbf	tbf	mA
V_{DD3}	supply voltage (3 V) range		3	3.3	3.6	V
I_{DD3}	V_{DD3} supply current		–	tbf	tbf	mA
$I_{DD(tot)}$	total supply current		–	tbf	tbf	mA
Digital inputs						
ALL INPUTS (EXCEPT $\overline{\text{RESET}}$ AND OSCILLATOR INPUTS)						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
$\overline{\text{RESET}}$ INPUT: (SCHMITT INPUT)						
V_{IL}	LOW level input voltage		–0.3		+2	V
V_{IH}	HIGH level input voltage		3.5		V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10		+10	µA
V_{hys}	hysteresis voltage ($V_{IH} - V_{IL}$)		1	–	–	V
Inputs/outputs						
SDA AND SCL (I^2C-BUS DATA AND CLOCK)						
V_{IL}	LOW level input voltage		–0.5	–	+1.5	V
V_{IH}	HIGH level input voltage		3	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	400	pF
V_{OL}	LOW level output voltage	(I_{OL} = 3.0 mA)	0	–	0.4	V
V_{OL}	LOW level output voltage	(I_{OL} = 6.0 mA)	0	–	0.6	V
CLK27						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.4	–	V_{DD} + 0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	(I_{OL} = 1.6 mA)	0	–	0.4	V
V_{OH}	HIGH level output voltage	(I_{OH} = –0.2 mA)	2.6	–	V_{DD}	V
t_r	input rise time	0.6 to 2.6 V	–	–	4	ns
t_f	input fall time	0.6 to 2.6 V	–	–	4	ns
DR15 TO DR0 (DRAM DATA I/O)						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	30	pF
V_{OL}	LOW level output voltage	(I_{OL} = 1.6 mA)	0	–	0.4	V
V_{OH}	HIGH level output voltage	(I_{OH} = –0.2 mA)	2.4	–	V_{DD}	V
t_r	output rise time	0.6 to 2.6 V; load = C_L	3	–	10	ns
t_f	output fall time	0.6 to 2.6 V; load = C_L	3	–	10	ns
Outputs						
$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, A0 TO A8 (DRAM CONTROL AND ADDRESS LINES)						
V_{OL}	LOW level output voltage	(I_{OL} = 1.6 mA)	0	–	0.4	V
V_{OH}	HIGH level output voltage	(I_{OH} = –0.2 mA)	2.4	–	V_{DD}	V
C_L	load capacitance			–	30	pF
t_r	output rise time	0.6 to 2.2 V; load = C_L	3	–	10	ns
t_f	output fall time	0.6 to 2.2 V; load = C_L	3	–	10	ns
Y0 TO Y7 (VIDEO OUTPUT Y BUS)						
V_{OL}	LOW level output voltage	(I_{OL} = 1.6 mA)	0	–	0.4	V
V_{OH}	HIGH level output voltage	(I_{OH} = –0.2 mA)	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.6 to 2.6 V; load = C_L	–	–	4	ns
t_f	output fall time	0.6 to 2.6 V; load = C_L	–	–	4	ns
UV0 TO UV7 (VIDEO OUTPUT UV BUS)						
V_{OL}	LOW level output voltage	(I_{OL} = 1.6 mA)	0	–	0.4	V
V_{OH}	HIGH level output voltage	(I_{OH} = -0.2 mA)	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.6 to 2.2 V; load = C_L	–	–	10	ns
t_f	output fall time	0.6 to 2.2 V; load = C_L	3	–	10	ns
$\overline{INT}$ (OPEN DRAIN; INTERRUPT)						
V_{OL}	LOW level output voltage	(I_{OL} = 1.6 mA)	0	–	0.4	V
C_L	load capacitance		–	–	30	pF
t_r	output rise time	0.6 to 2.2 V; load = C_L	–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_f	output fall time	0.6 to 2.2 V; load = C_L	–	–	10	ns
EBUOUT (IEC 958 OUT)						
V_{OL}	LOW level output voltage	(I_{OL} = 10 mA)	0	–	1	V
V_{OH}	HIGH level output voltage	(I_{OH} = –10 mA)	V_{DD5}–1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD5} – 0.8 V); load = C_L	–	–	10	ns
t_r	output fall time	0.8 V to (V_{DD5} – 0.8 V); load = C_L	–	–	10	ns
ALL OTHER INPUTS						
V_{OL}	LOW level output voltage	(I_{OL} = 1.6 mA)	0	–	0.4	V
V_{OH}	HIGH level output voltage	(I_{OH} = –0.2 mA)	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 to 2.6 V; load = C_L	–	–	30	ns
t_f	output fall time	0.6 to 2.6 V; load = C_L	–	–	30	ns
I^2S input/output timing; (Fig.5)						
INPUT TIMING						
f_{clk}	input clock frequency		–	2.118	–	MHz
t_{clkH}	input clock HIGH period		166	–	–	ns
t_{clkL}	input clock LOW period		166	–	–	ns
t_{su}	set-up time (DAIN, EFIN, WSIN)		95	–	–	ns
t_{h1}	hold time DAIN, EFIN, WSIN)		0	–	–	ns
OUTPUT TIMING						
f_{clk}	output clock frequency		–	2.118	–	MHz
t_{clkH}	output clock HIGH period		166	–	–	ns
t_{h2}	hold time (DAOUT, WSOUT)		195	–	–	ns
t_d	output delay time (DAOUT, WSOUT)		–	–	147	ns
I^2C-bus input/output timing (Fig.6)						
100 kHz CLOCK FREQUENCY						
f_{clk}	clock frequency		0	–	100	kHz
t_{LOW}	clock LOW period		4.7	–	–	µs
t_{HIGH}	period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time clock HIGH to STOP		4.7	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{BUF}	set-up time STOP to START		4.7	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	set-up time clock rising edge to START		4.7	–	–	µs
t_r	rise time (SDA and SCL)	V_{ILmin} to V_{IHmax}	50	–	1000	ns
t_f	fall time (SDA and SCL)	V_{ILmin} to V_{IHmax}	50	–	300	ns
400 kHz CLOCK FREQUENCY						
f_{clk}	clock frequency		0	–	400	kHz
t_{LOW}	clock LOW period		1.3	–	–	µs
t_{HIGH}	period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time clock HIGH to STOP		0.6	–	–	µs
t_{BUF}	set-up time STOP to START		1.3	–	–	µs
$t_{HD;STA}$	START hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time clock rising edge to START		0.6	–	–	µs
t_r	rise time (SDA and SCL)	V_{ILmin} to V_{IHmax}	50	–	300	ns
t_f	fall time (SDA and SCL)	V_{ILmin} to V_{IHmax}	50	–	300	ns
Video Output Timing (Figs. 7 and 8)						
16-BIT VIDEO OUTPUT MODE						
t_{su}	set-up time (CREF, HREF, UV and Y valid to CLK27)		10	–	–	ns
t_{h2}	hold time (CLK27 to CREF, HREF, UV and Y invalid)		3	–	–	ns
t_{su}	set-up time (UV and Y valid to CREF rising edge)		6	–	–	ns
t_{h1}	hold time (CREF rising edge to UV and Y invalid)		10	–	–	ns
8-BIT VIDEO OUTPUT MODE						
t_{su}	set-up time (HREF and Y valid to CLK27)		7	–	–	ns
t_{h2}	hold time (CLK27 to HREF and Y invalid)		5	–	–	ns
DRAM Timing (Fig.9)						
t_{CYC}	cycle time		130	–	–	ns
t_{RP}	$\overline{RAS}$ pre-charge time		50	–	–	ns
t_{CSH}	$\overline{CAS}$ hold time		70	–	–	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		20	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{CAS}	$\overline{CAS}$ pulse width LOW		20	–	–	ns
t_{PC}	page mode cycle time		50	–	–	ns
t_{CP}	$\overline{CAS}$ pre-charge time		10	–	–	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		20	–	–	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ pre-charge time		15	–	–	ns
t_{ASR}	row address set-up time		0	–	–	ns
t_{RAH}	row address hold time		10	–	–	ns
t_{ASC}	column address set-up time		0	–	–	ns
t_{CAH}	column address hold time		15	–	–	ns
t_{RCS}	read command set-up time		0	–	–	ns
t_{RCH}	read command hold time ($\overline{CAS}$)		0	–	–	ns
t_{RRH}	read command hold time ($\overline{RAN}$)		0	–	–	ns
t_{WCS}	write command set-up time		0	–	–	ns
t_{WCH}	write command hold time		15	–	–	ns
t_{DS}	data-in set-up time		0	–	–	ns
t_{DH}	data-in hold time		15	–	–	ns
t_{CAC}	read access time ($\overline{CAS}$)		–	–	20	ns
t_{RAC}	read access time ($\overline{RAS}$)		–	–	70	ns
Crystal oscillators						
40 MHz SYSTEM CLOCK OSCILLATOR						
$V_{osc(p-p)}$	oscillation amplitude (peak-to-peak)		–	tbf	–	V
G_v	small signal voltage gain		–	tbf	–	
G_m	mutual conductance		tbf	–	–	mA/V
C_i	input capacitance		–	–	tbf	pF
C_{fb}	feedback capacitance		–	tbf	–	pF
f_{OSC}	oscillation frequency		–	40	–	MHz
Δf	frequency tolerance		–	–	–	ppm
27 MHz SYSTEM CLOCK OSCILLATOR						
$V_{osc(p-p)}$	oscillation amplitude (peak-to-peak)		–	tbf	–	V
G_V	small signal voltage gain		–	tbf	–	
G_m	mutual conductance		tbf	–	–	mA/V
C_i	input capacitance		–	–	tbf	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{fb}	feedback capacitance		–	tbf	–	pF
f_{osc}	oscillation frequency		–	27	–	MHz
Δf	frequency tolerance		–	–	–	ppm

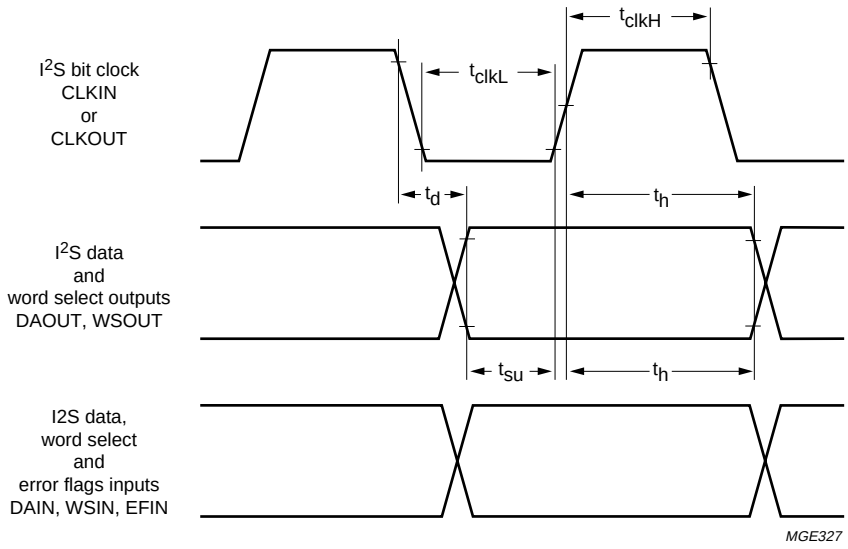


Fig.5 I^2S input/output timing.

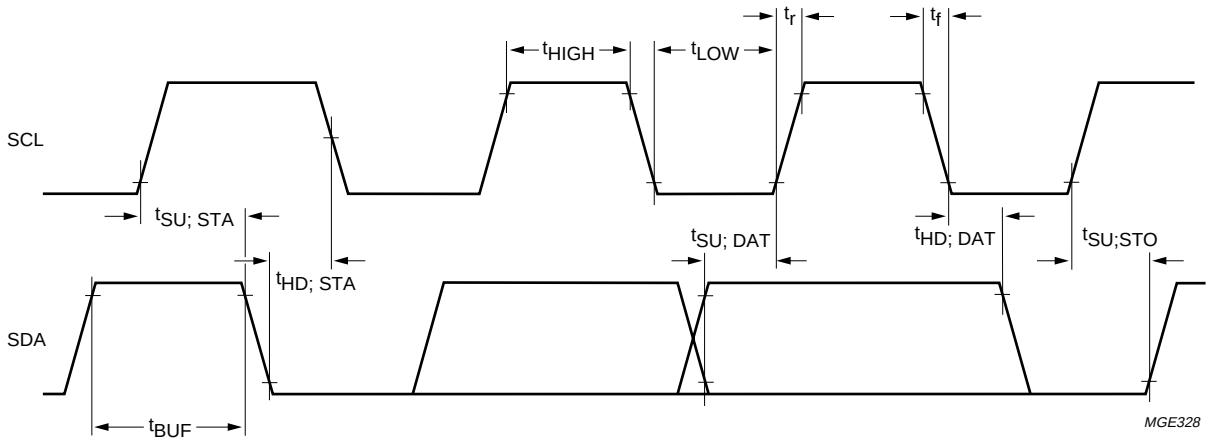
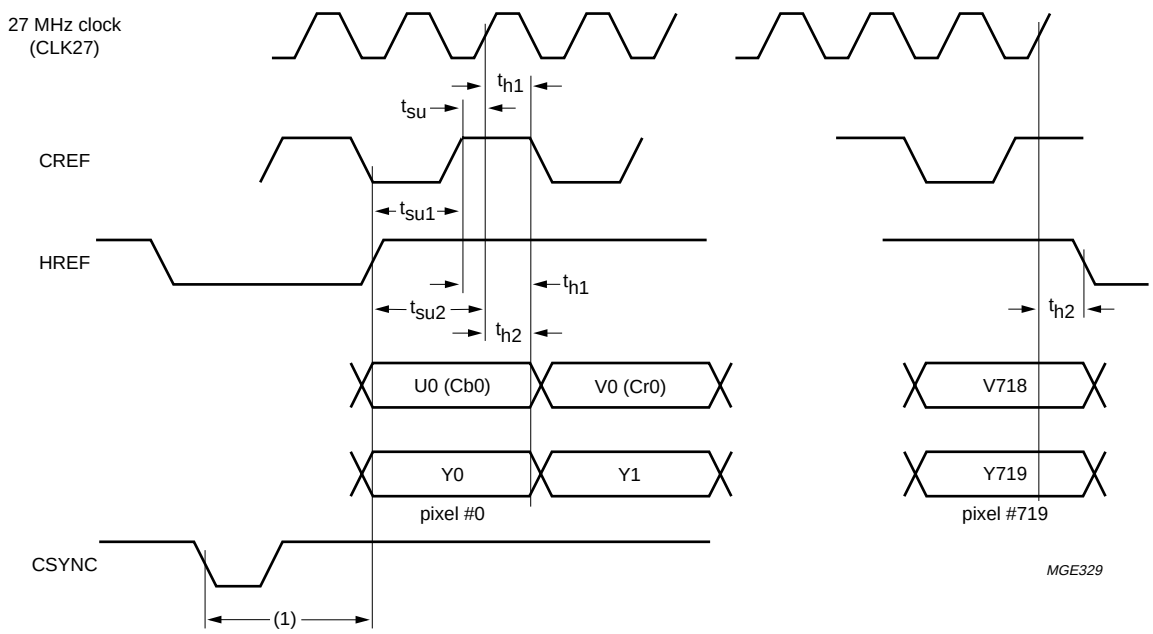


Fig.6 I^2C-bus timing.



Timing applies to CLK27 when programmed as an input or an output of the SAA2510.

(1) CSYNC (HIGH-to-LOW) to first sample and HREF (LOW-to-HIGH) = 264.5/244.5 CLK27 periods (625 lines/525 lines mode).

Fig.7 16-bit video output mode timing.

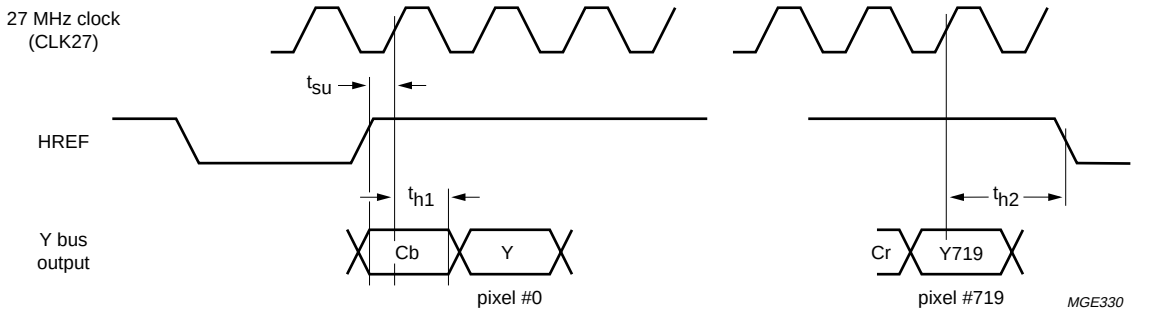


Fig.8 8-bit video CCIR656 output mode timing.

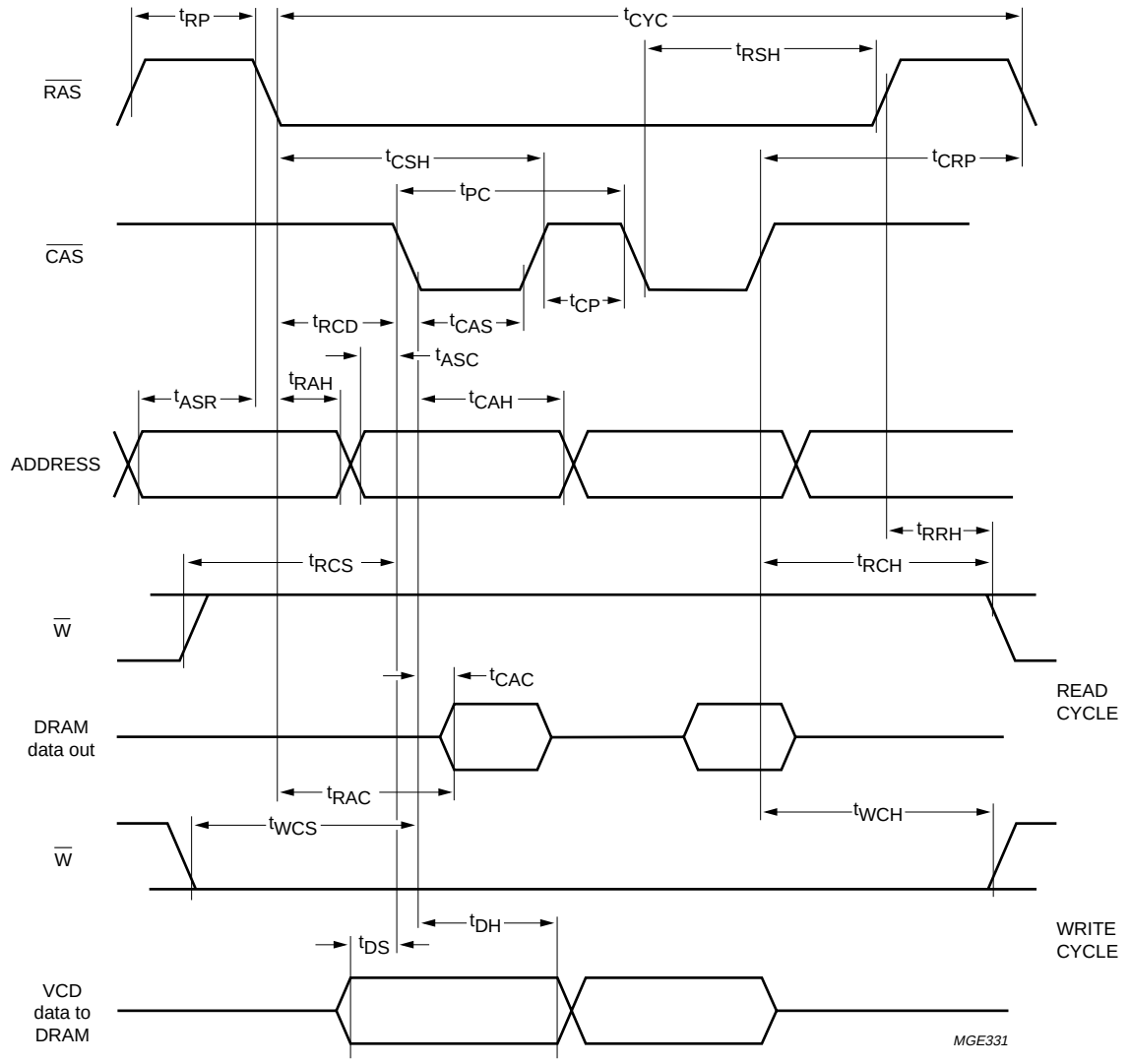
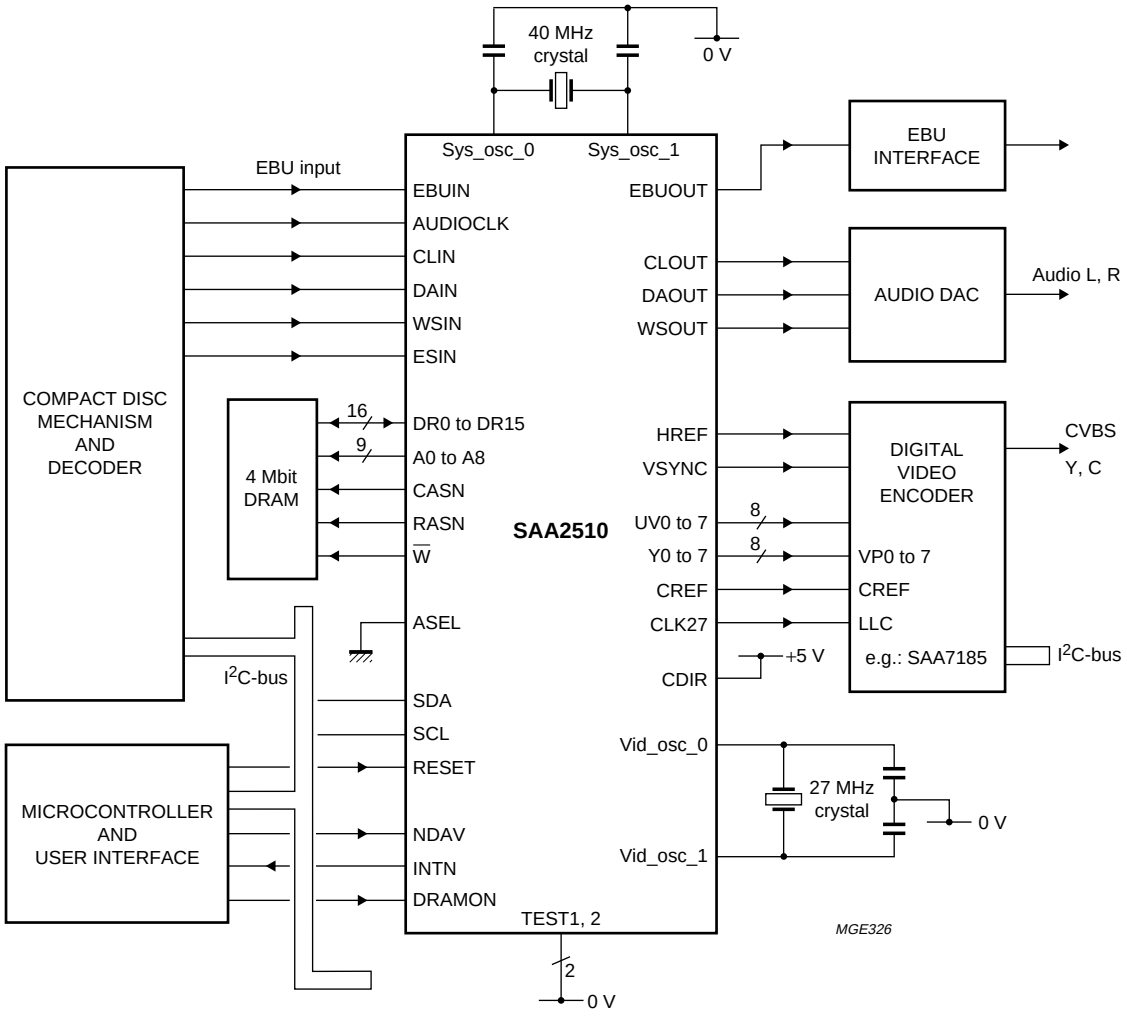


Fig.9 DRAM timing.

APPLICATION INFORMATION

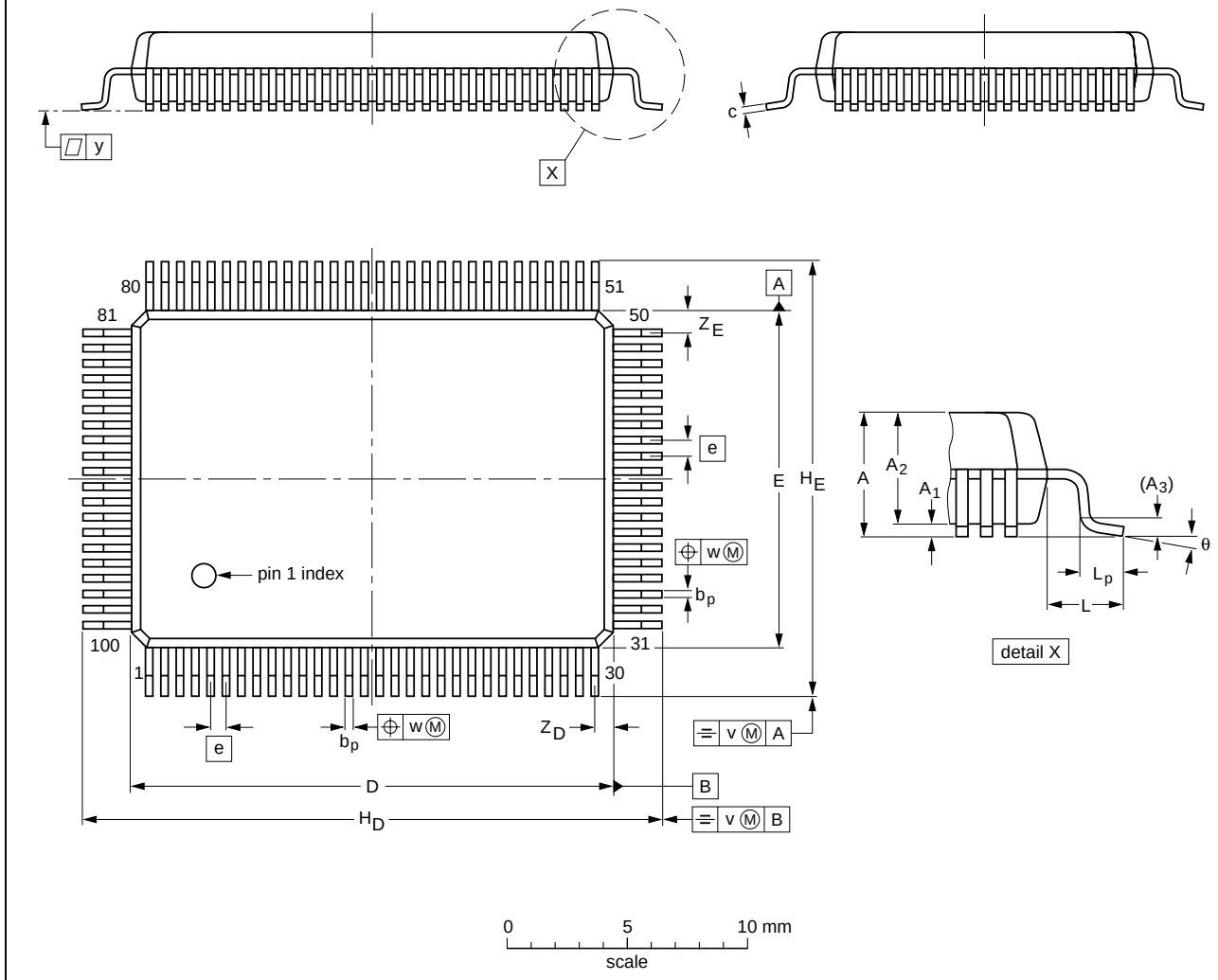


VCD power supply pins not shown.

Fig.10 Application diagram; 16-bit video output mode.

PACKAGE OUTLINE

QFP100: plastic quad flat package;
100 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT317-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.40 0.25	0.25 0.13	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-1						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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